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Figure 1A
(PRIOR ART)

Figure 1B
(PRIOR ART)

(WITHOUT CHARGE)

Figure 1C
(PRIOR ART)

(WITH CHARGE)

Figure 1D
(PRIOR ART)

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CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	31536000	1 year
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	94608000	3 years
					1.9E+008	6 years
b0, eV (barrier)	εl	mr, effective mass ratio		T, K degree	2.8E+017	9 years
2.9	3.9	0.5		300	3.8E+008	12 years
					4.7E+008	15 years
C	b				9.1E+009	18 years
1.0630E-006	2.3854E+008				6.6E+008	21 years
					7.6E+008	24 years
					8.5E+008	27 years
					9.5E+008	30 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1078	Capacitance between the floating gate and the drain
Cfs fF	0.7547	Capacitance between the floating gate and the source
Cfg fF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation

Figure 1E
(PRIOR ART)

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t, sec.	Vt,fg
0.00001	5.907
31536000	5.894
63072000	5.882
94608000	5.871
1.3E+008	5.861
1.6E+008	5.852
1.9E+008	5.843
2.2E+008	5.835
2.5E+008	5.827
2.8E+008	5.820
3.2E+008	5.814
3.5E+008	5.807
3.8E+008	5.801
4.1E+008	5.795
4.4E+008	5.790
4.7E+008	5.785
5E+008	5.780
5.4E+008	5.775
5.7E+008	5.770
6E+008	5.766
6.3E+008	5.762
6.6E+008	5.757
6.9E+008	5.753
7.3E+008	5.750
7.6E+008	5.746
7.9E+008	5.742
8.2E+008	5.739
8.5E+008	5.735
8.8E+008	5.732
9.1E+008	5.729
9.5E+008	5.726

FLOATING DEVICE Vt vs. TIME

Figure 1F
(PRIOR ART)

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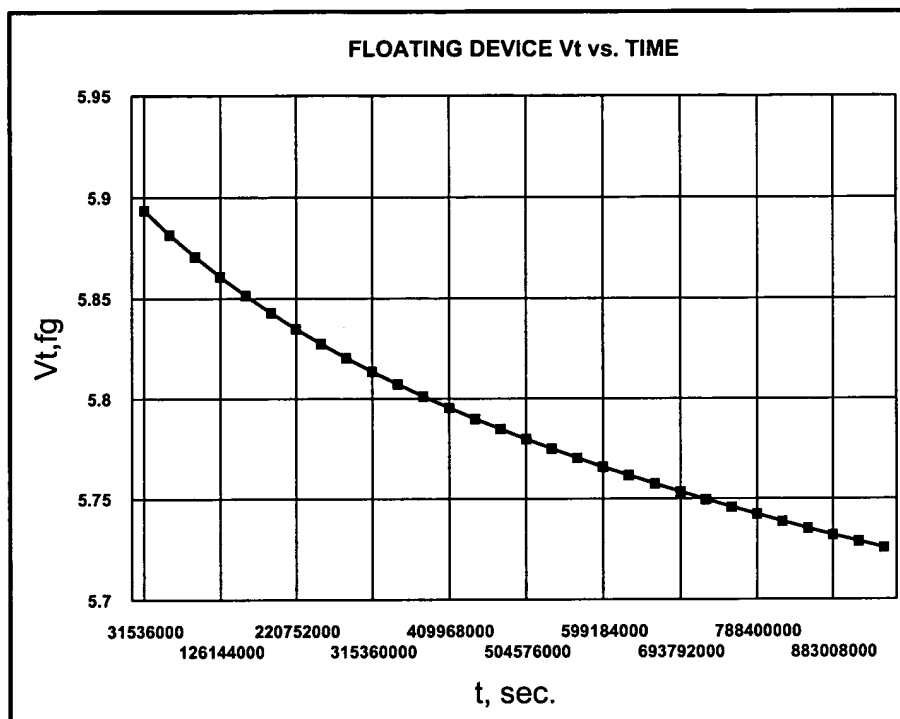**Batteryless, oscillatorless, analog time cell usable as an horological device**
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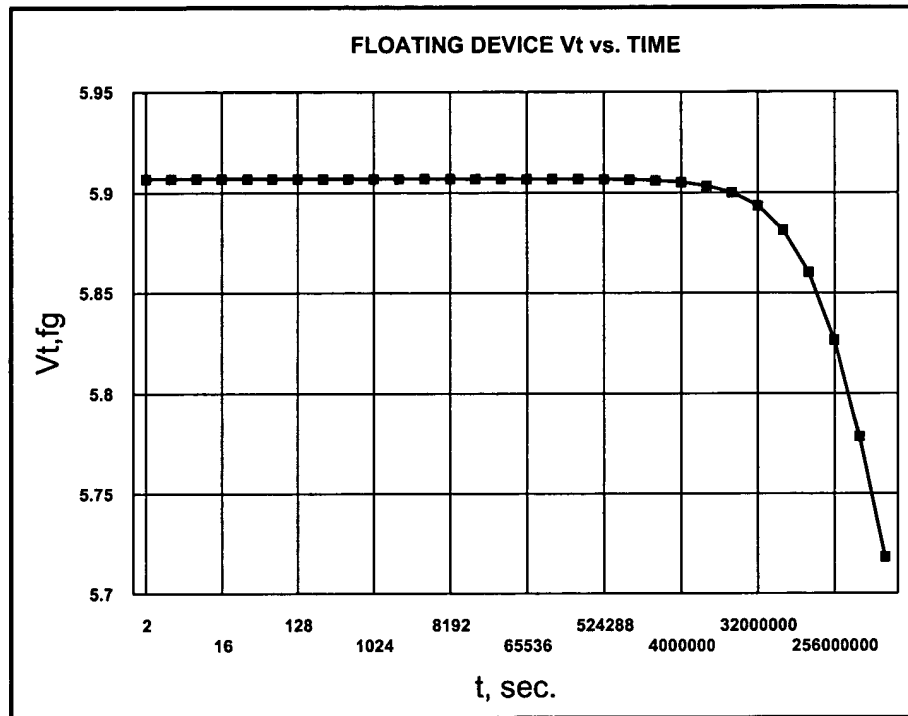## CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	ε1	mr, effective mass ratio		T, K degree	604800	1 week
2.9	3.9	0.5		300	2592000	1 month
					31536000	1 year
C	b				1.3E+008	4 years
1.0630E-006	2.3854E+008				5E+008	16 years
					1E+009	32 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1078	Capacitance between the floating gate and the drain
Cfs fF	0.7547	Capacitance between the floating gate and the source
Cfg fF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation

Figure 1G
(PRIOR ART)

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t, sec.	Vt,fg
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.906
4000000	5.905
8000000	5.904
16000000	5.900
32000000	5.894
64000000	5.881
1.3E+008	5.860
2.6E+008	5.827
5.1E+008	5.779
1E+009	5.718

Figure 1H
(PRIOR ART)

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CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	εl	mr, effective mass ratio		T, K degree	604800	1 week
2.9	3.9	0.5		300	2592000	1 month
					31536000	1 year
C	b				1.3E+008	4 years
1.0630E-006	2.3854E+008				5E+008	16 years
					1E+009	32 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	85	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4059	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1015	Capacitance between the floating gate and the drain
Cfs fF	0.7103	Capacitance between the floating gate and the source
Cfg fF	1090.7534	Total floating gate capacitance
Cr,wl	0.9989	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio

Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	4.09E+017	Derived parameter in the floating gate "erase" equation
X	1.20E+011	Derived parameter in the floating gate "erase" equation

Figure 1I
(PRIOR ART)

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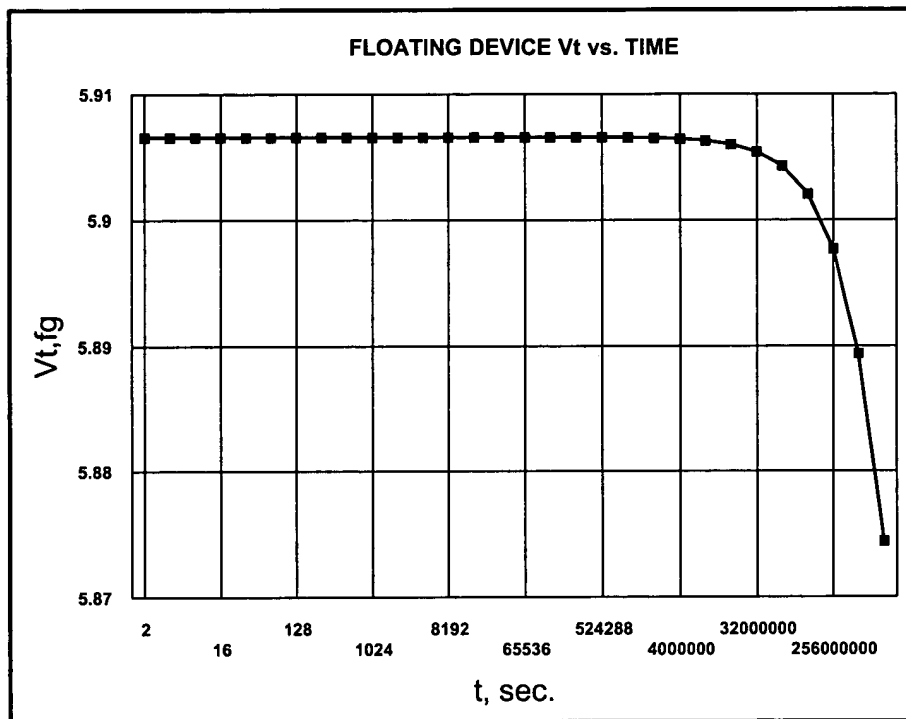with associated programming methods and devices

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t, sec.	Vt,fg
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.907
4000000	5.906
8000000	5.906
16000000	5.906
32000000	5.905
64000000	5.904
1.3E+008	5.902
2.6E+008	5.898
5.1E+008	5.889
1E+009	5.874

Figure 1J
(PRIOR ART)

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Figure 1K

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CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	2592000	1 month
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	5184000	2 months
					7776000	3 months
b0, eV (barrier)	εl	mr, effective mass ratio		T, K degree	10368000	4 months
2.9	3.9	0.5		300	12960000	5 months
					15552000	6 months
C	b				18144000	7 months
1.0630E-006	2.3854E+008				20736000	8 months
					23328000	9 months
					25920000	10 months
					28512000	11 months
					31104000	12 months

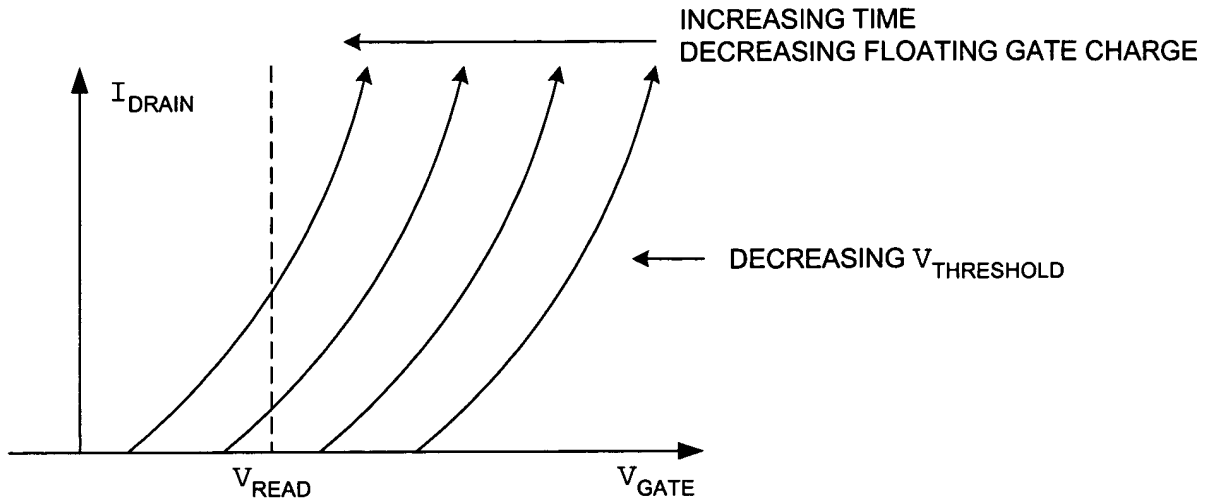|				
Lfg um	0.6000	Channel length of floating gate device	33696000	13 months
Wfg um	1000.0000	Channel width of floating gate device.	36288000	14 months
Hfg um	0.0900	Thickness of floating gate polysilicon conductor	38880000	15 months
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation	41472000	16 months
Ttunox A	65	Tunnel oxide thickness		
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling		
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling		
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET		
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET		
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge		
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate		
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate		
Cfd fF	0.1327	Capacitance between the floating gate and the drain		
Cfs fF	0.9288	Capacitance between the floating gate and the source		
Cfg fF	1091.1281	Total floating gate capacitance		
Cr,wl	0.9985	Control gate to floating gate coupling ratio		
Cr,src	0.0009	Source junction to floating gate coupling ratio		
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET		
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)		
Vfg,ini	-5.00	Initial floating chaged voltage		
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)		
S	2.93E+013	Derived parameter in the floating gate "erase" equation		
X	1.56E+011	Derived parameter in the floating gate "erase" equation		

Figure 1L

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t, sec.	Vt,fg
0.00001	5.909
1296000	5.596
2592000	5.508
3888000	5.456
5184000	5.420
6480000	5.392
7776000	5.369
9072000	5.349
10368000	5.333
11664000	5.318
12960000	5.305
14256000	5.293
15520000	5.283
16848000	5.273
18144000	5.264
19440000	5.256
20736000	5.248
22032000	5.240
23328000	5.234
24624000	5.227
25920000	5.221
27216000	5.215
28512000	5.210
29808000	5.204
31104000	5.199
32400000	5.195
33696000	5.190
34992000	5.185
36288000	5.181
37584000	5.177
38880000	5.173

FLOATING DEVICE Vt vs. TIME

Figure 1M

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CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	ε1	mr, effective mass ratio		T, K degree	604800	1 week
2.9	3.9	0.5		300	1209600	2 weeks
					2592000	1 month
C	b				5184000	2 months
1.0630E-006	2.3854E+008				10368000	4 months
					15552000	6 months
					20736000	8 months
					25920000	10 months
					31104000	12 months

			Seconds	Time Period
Lfg um	0.6000	Channel length of floating gate device	36288000	14 months
Wfg um	1000.0000	Channel width of floating gate device.	41472000	16 months
Hfg um	0.0900	Thickness of floating gate polysilicon conductor		
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation		
Ttunox A	65	Tunnel oxide thickness		
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling		
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling		
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET		
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET		
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge		
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate		
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate		
Cfd fF	0.1327	Capacitance between the floating gate and the drain		
Cfs fF	0.9288	Capacitance between the floating gate and the source		
Cfg fF	1091.1281	Total floating gate capacitance		
Cr,wl	0.9985	Control gate to floating gate coupling ratio		
Cr,src	0.0009	Source junction to floating gate coupling ratio		
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET		
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)		
Vfg,ini	-5.00	Initial floating chaged voltage		
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)		
S	2.93E+013	Derived parameter in the floating gate "erase" equation		
X	1.56E+011	Derived parameter in the floating gate "erase" equation		

Figure 1N

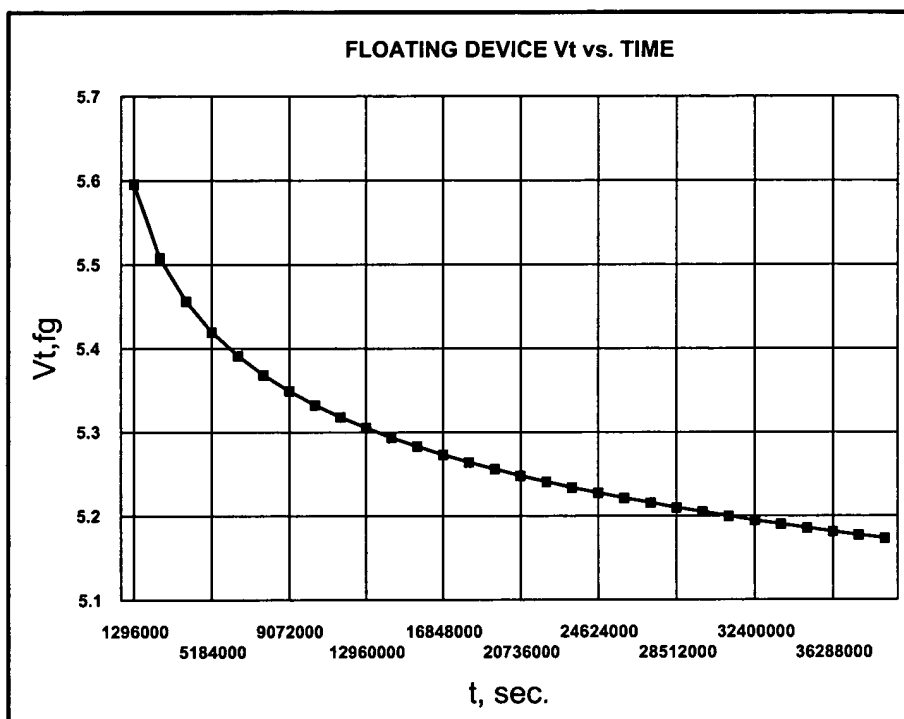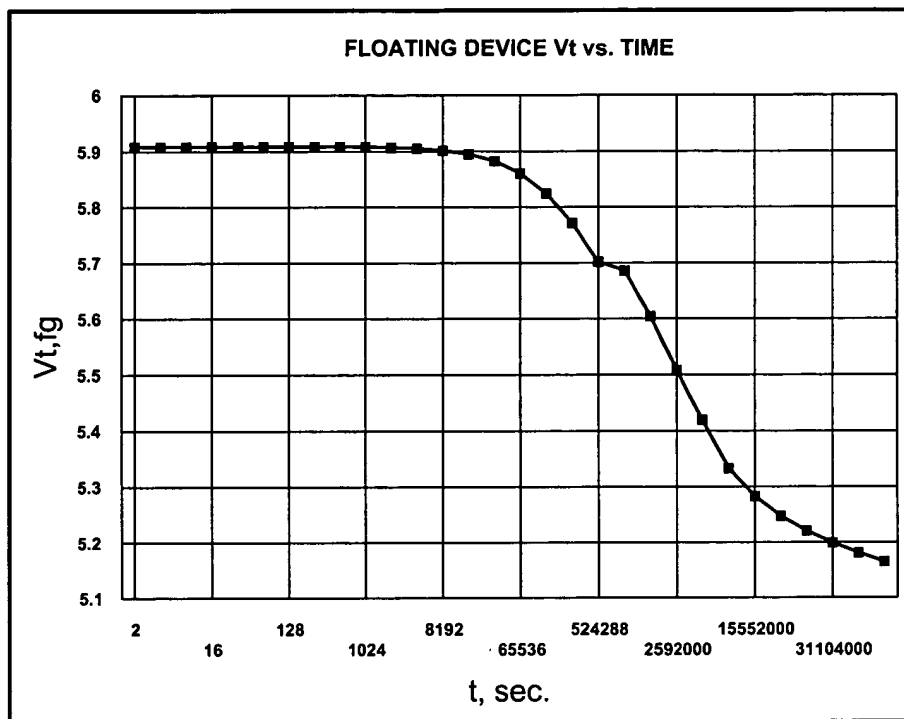U.S. Serial Number 09/703,335   Atty. Docket # AUS9-1999-0269-US1
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t, sec.	Vt,fg
0.00001	5.909
2	5.909
4	5.909
8	5.909
16	5.909
32	5.909
64	5.909
128	5.909
256	5.908
512	5.908
1024	5.908
2048	5.907
4096	5.905
8192	5.902
16384	5.895
32768	5.883
65536	5.861
131072	5.824
262144	5.771
524288	5.702
604800	5.686
1209600	5.604
2592000	5.508
5184000	5.420
10368000	5.333
15552000	5.283
20736000	5.248
25920000	5.221
31104000	5.199
36288000	5.181
41472000	5.166

FLOATING DEVICE Vt vs. TIME

Vt,fg

t, sec.

Figure 10

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CALCULATION OF NV MEMORY CELL RETENTION CHARACTERISTICS

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.05459E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	εl	mr, effective mass ratio		T, K degree	604800	1 week
2.9	3.9	0.5		300	1209600	2 weeks
					2592000	1 month
C	b				5184000	2 months
1.0630E-006	2.3854E+008				10368000	4 months
					15552000	6 months
					20736000	8 months
					25920000	10 months
					31104000	12 months
Lfg um	0.6000	Channel length of floating gate device			36288000	14 months
Wfg um	1000.0000	Channel width of floating gate device.			41472000	16 months

Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	60	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.5750	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1438	Capacitance between the floating gate and the drain
Cfs fF	1.0063	Capacitance between the floating gate and the source
Cfg fF	1091.2608	Total floating gate capacitance
Cr,wl	0.9984	Control gate to floating gate coupling ratio
Cr,src	0.0009	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating chaged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	2.70E+012	Derived parameter in the floating gate "erase" equation
X	1.69E+011	Derived parameter in the floating gate "erase" equation

Figure 1P

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t, sec.	Vt,fg
0.00001	5.909
2	5.909
4	5.909
8	5.909
16	5.909
32	5.909
64	5.909
128	5.908
256	5.907
512	5.904
1024	5.898
2048	5.888
4096	5.870
8192	5.838
16384	5.789
32768	5.721
65536	5.639
131072	5.549
262144	5.455
524288	5.360
604800	5.341
1209600	5.250
2592000	5.152
5184000	5.067
10368000	4.985
15552000	4.938
20736000	4.906
25920000	4.881
31104000	4.861
36288000	4.844
41472000	4.830

FLOATING DEVICE Vt vs. TIME

Figure 1Q

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PROGRAMMING
REQUEST SIGNAL
206

CHARGE STORAGE ELEMENT
222

200

PROGRAMMING
STATUS
SIGNAL
212

INSULATING
MEDIUM
220

TIME DETECTION UNIT
230

PROGRAMMING UNIT
202

INTERNAL
MEDIUM
WITH
CHARGE-
BEARING
CAPABILITY
224

ELECTRIC
FIELD
228

ELECTROSTATIC
DETECTOR
236

CHARGE
GENERATOR
208

POTENTIAL-TO-
TIME CONVERTER
238

CHARGE
PROCESS
210

ELAPSED
TIME
SIGNAL
240

DISCHARGE
PROCESS
226

ELECTRICAL
POWER SUPPLY A
204

ELECTRICAL
POWER SUPPLY B
232

TIME
MEASUREMENT
REQUEST
SIGNAL
234

Figure 2A

BEGIN

SEND PROGRAMMING REQUEST
TO PROGRAMMING UNIT
252

RECEIVE PROGRAMMING STATUS
FROM PROGRAMMING UNIT
254

END

Figure 2B

BEGIN

SEND TIME MEASUREMENT REQUEST
TO TIME DETECTION UNIT
262

RECEIVE ELAPSED TIME VALUE
FROM TIME DETECTION UNIT
264

END

Figure 2C

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PROGRAMMING
REQUEST
PROCESSING
UNIT
322

↑ INITIALIZATION REQUEST
324

○

TIME CELL
INTERFACE
UNIT
320

[1 WEEK]
TIME CELL #0
301

[2 WEEKS]
TIME CELL #1
302

[3 WEEKS]
TIME CELL #2
303

[4 WEEKS]
TIME CELL #3
304

[5 WEEKS]
TIME CELL #4
305

[6 WEEKS]
TIME CELL #5
306

[7 WEEKS]
TIME CELL #6
307

[8 WEEKS]
TIME CELL #7
308

[3 MONTHS]
TIME CELL #8
309

[4 MONTHS]
TIME CELL #9
310

[5 MONTHS]
TIME CELL #10
311

[6 MONTHS]
TIME CELL #11
312

[9 MONTHS]
TIME CELL #12
313

[12 MONTHS]
TIME CELL #13
314

[15 MONTHS]
TIME CELL #14
315

[18 MONTHS]
TIME CELL #15
316

○

TIME
DETECTION
UNIT
326

← TIME REQUEST
328

Figure 3A

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```
┌─────────────────┐
│  TIME SET       │     ┌──────────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐
│  IDENTIFIER     │     │  [1 WEEK]    │  │  [2 WEEKS]   │  │  [3 WEEKS]   │  │  [4 WEEKS]   │
│  UNIT           │     │  TIME CELL #0│  │  TIME CELL #1│  │  TIME CELL #2│  │  TIME CELL #3│
│  348            │     │     331      │  │     332      │  │     333      │  │     334      │
└─────────────────┘     └──────────────┘  └──────────────┘  └──────────────┘  └──────────────┘

                        ┌──────────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐
                        │  [1 WEEK]    │  │  [2 WEEKS]   │  │  [3 WEEKS]   │  │  [4 WEEKS]   │
  TIME CELL             │  TIME CELL #4│  │  TIME CELL #5│  │  TIME CELL #6│  │  TIME CELL #7│
  INTERFACE             │     335      │  │     336      │  │     337      │  │     338      │
  UNIT                  └──────────────┘  └──────────────┘  └──────────────┘  └──────────────┘
  330
                        ┌──────────────┐  ┌──────────────┐  ┌───────────────┐  ┌───────────────┐
                        │  [2 MONTHS]  │  │  [4 MONTHS]  │  │  [6 MONTHS]   │  │  [8 MONTHS]   │
                        │ TIME CELL #8 │  │ TIME CELL #9 │  │ TIME CELL #10 │  │ TIME CELL #11 │
                        │     339      │  │     340      │  │     341       │  │     342       │
                        └──────────────┘  └──────────────┘  └───────────────┘  └───────────────┘

                        ┌───────────────┐  ┌───────────────┐  ┌───────────────┐  ┌───────────────┐
                        │  [2 MONTHS]   │  │  [4 MONTHS]   │  │  [6 MONTHS]   │  │  [8 MONTHS]   │
                        │ TIME CELL #12 │  │ TIME CELL #13 │  │ TIME CELL #14 │  │ TIME CELL #15 │
                        │     343       │  │     344       │  │     345       │  │     346       │
                        └───────────────┘  └───────────────┘  └───────────────┘  └───────────────┘
```

Figure 3B

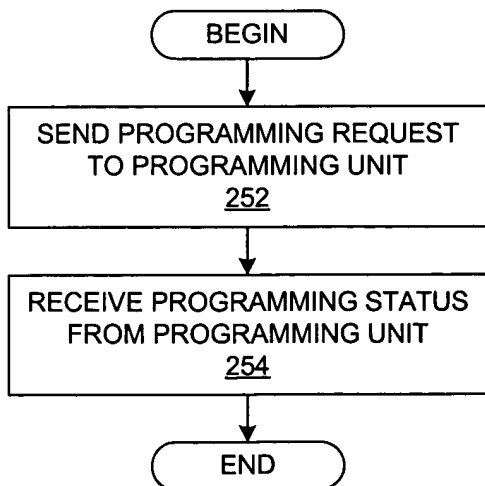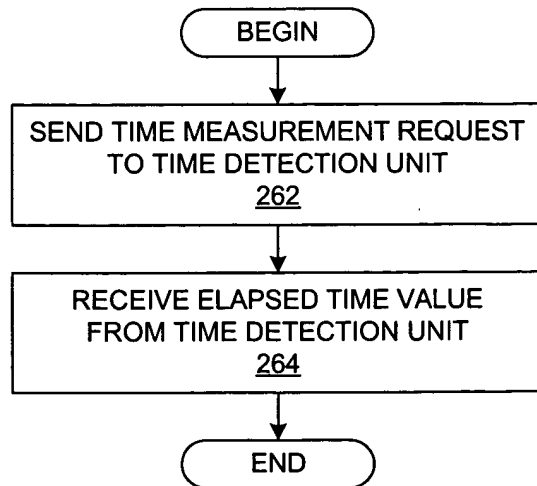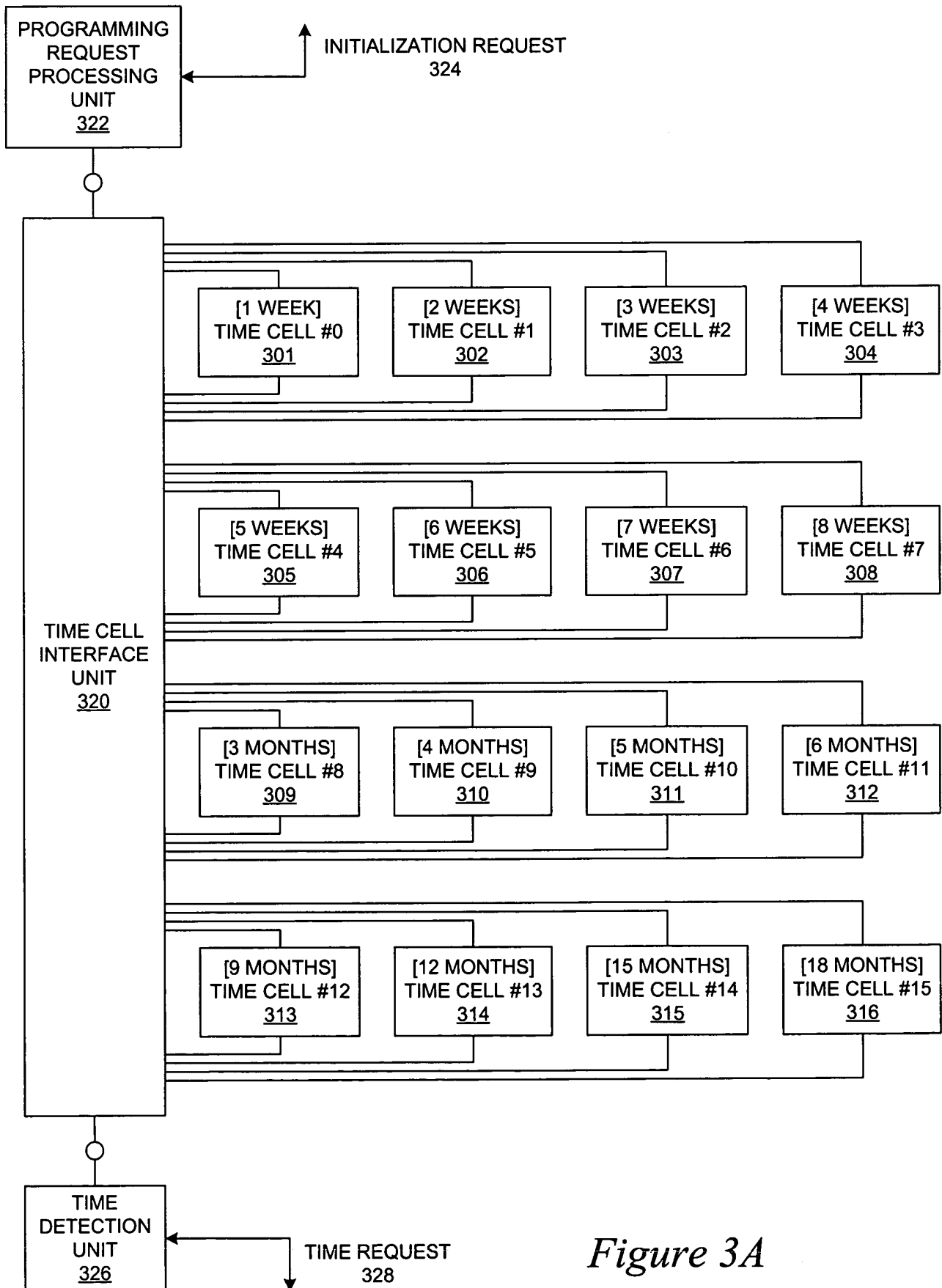**U.S. Serial Number 09/703,335   Atty. Docket # AUS9-1999-0269-US1**
Berstis et al.
Batteryless, oscillatorless, analog time cell usable as an horological device
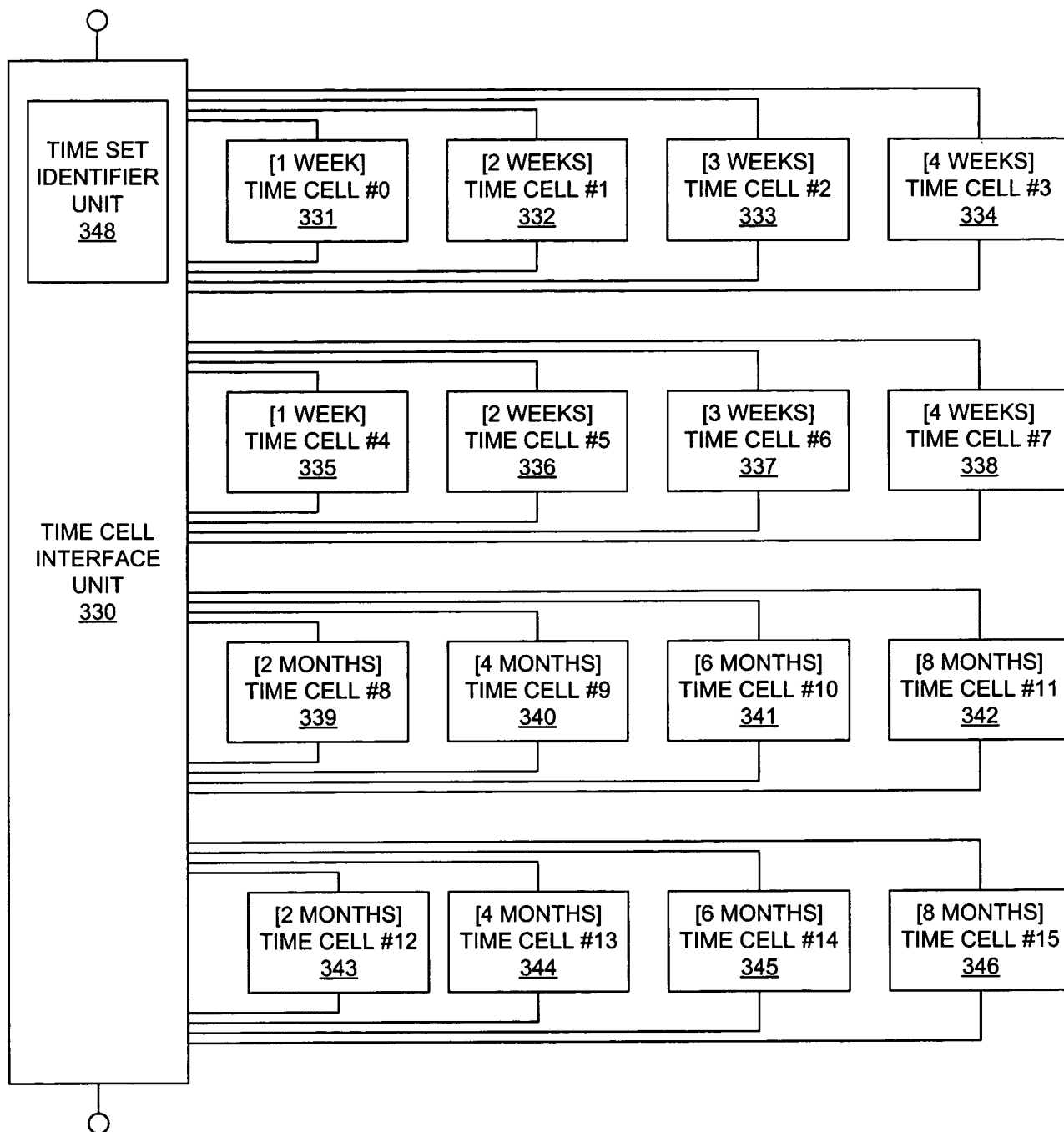**with associated programming methods and devices**

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TIME SET IDENTIFIER UNIT 368	[1 MONTH] TIME CELL #0 351	[1 MONTH] TIME CELL #1 352	[1 MONTH] TIME CELL #2 353	[1 MONTH] TIME CELL #3 354
TIME CELL INTERFACE UNIT 350	[1 MONTH] TIME CELL #4 355	[1 MONTH] TIME CELL #5 356	[1 MONTH] TIME CELL #6 357	[1 MONTH] TIME CELL #7 358
	[1 MONTH] TIME CELL #8 359	[1 MONTH] TIME CELL #9 360	[1 MONTH] TIME CELL #10 361	[1 MONTH] TIME CELL #11 362
	[1 MONTH] TIME CELL #12 363	[1 MONTH] TIME CELL #13 364	[1 MONTH] TIME CELL #14 365	[1 MONTH] TIME CELL #15 366

Figure 3C

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376

374

370

Figure 3D

CPU 381	NON-VOLATILE MEMORY 383	TIME CELL ARRAY 388	DISPLAY ADAPTER 384	DISPLAY 385
	BUTTON CONTROL UNIT 386	TIME CELL INTERFACE UNIT 389		
MEMORY 382	I/O INTERFACE UNIT 387			

380

Figure 3E

| PROGRAMMING UNIT 394 | TIME CELL(S) 395 | TIME DETECTION UNIT 396 |
| INITIALIZING DEVICE 391 | SMART CARD 392 | READING DEVICE 393 |

390

Figure 3F

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COMMON FLOATING GATE
406

CONTROL GATE
408

DRAIN
410

SOURCE
412

DRAIN
414

SOURCE
416

CONTROL GATE
418

PROGRAMMING FGFET
402

CHARGELOSS SENSING
FGFET
404

Figure 4A

COUPLING GATE
420

COMMON FLOATING GATE
406

CONTROL GATE
408

DRAIN
410

SOURCE
412

DRAIN
414

SOURCE
416

CONTROL GATE
418

PROGRAMMING FGFET
402

CHARGELOSS SENSING
FGFET
404

Figure 4B

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V_{CG}

V_{PD}

V_{PG}

PROGRAMMING FGFET

CHARGELOSS SENSING
FGFET

VOLTAGES DURING PROGRAMMING OPERATION

Figure 4C

V_{SS}

V_{SD}

V_{SG}

V_{SS}

PROGRAMMING FGFET

CHARGELOSS SENSING
FGFET

VOLTAGES DURING SENSING OPERATION

Figure 4D

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COMMON FLOATING
GATE

COUPLING
GATE

V_{PD}

V_{SD}

V_{PG}

V_{SG}

GROUND

V_{SS}

PROGRAMMING
FGFET

CHARGELOSS SENSING
FGFET

V_{CG}

Figure 4E

V_{CG}

| CONTACT |
| COUPLING GATE |
| INSULATING OXIDE |
| COMMON FLOATING GATE |
| INSULATING OXIDE |
| SUBSTRATE |

Figure 4F

U.S. Serial Number 09/703,335   Atty. Docket # AUS9-1999-0269-US1
Berstis et al.
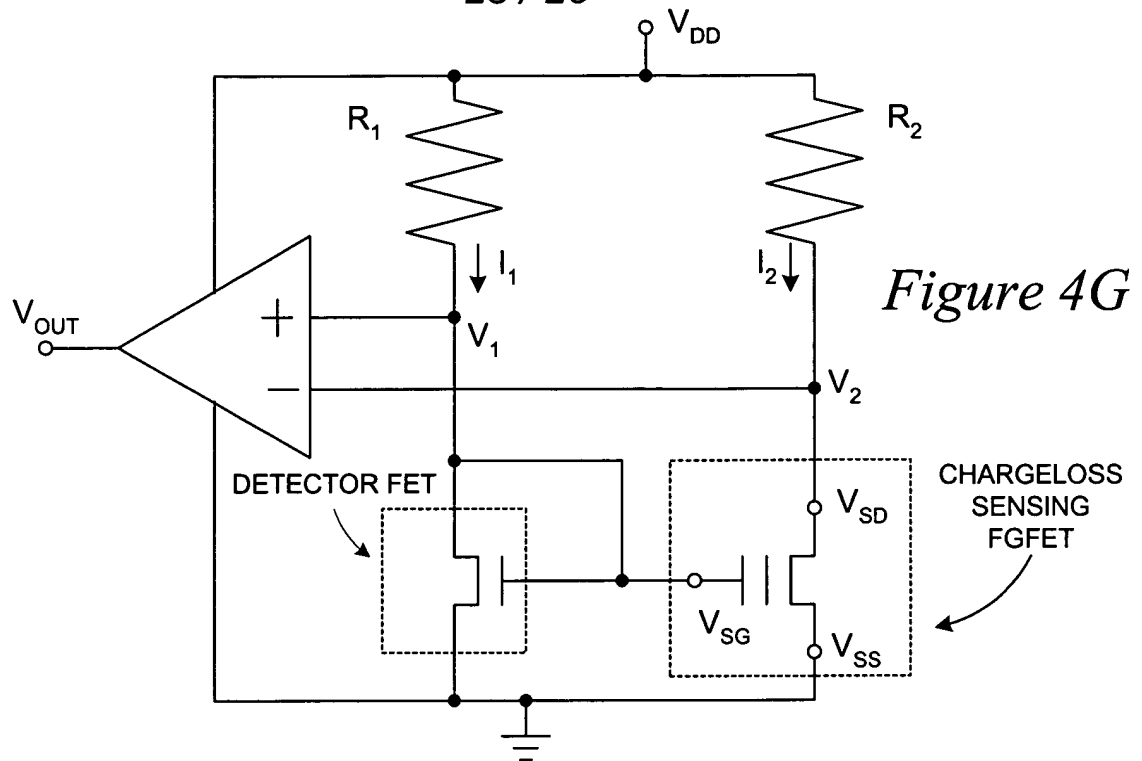Batteryless, oscillatorless, analog time cell usable as an horological device
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Figure 4G

Figure 4H

Figure 4I

Figure 4J

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Berstis et al.
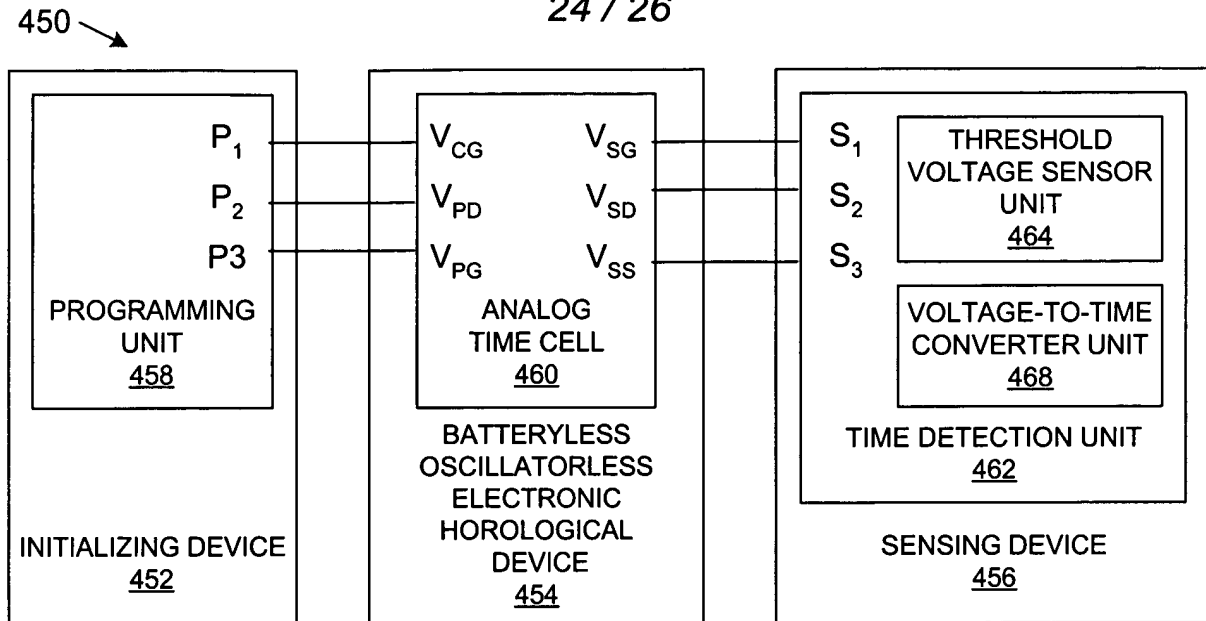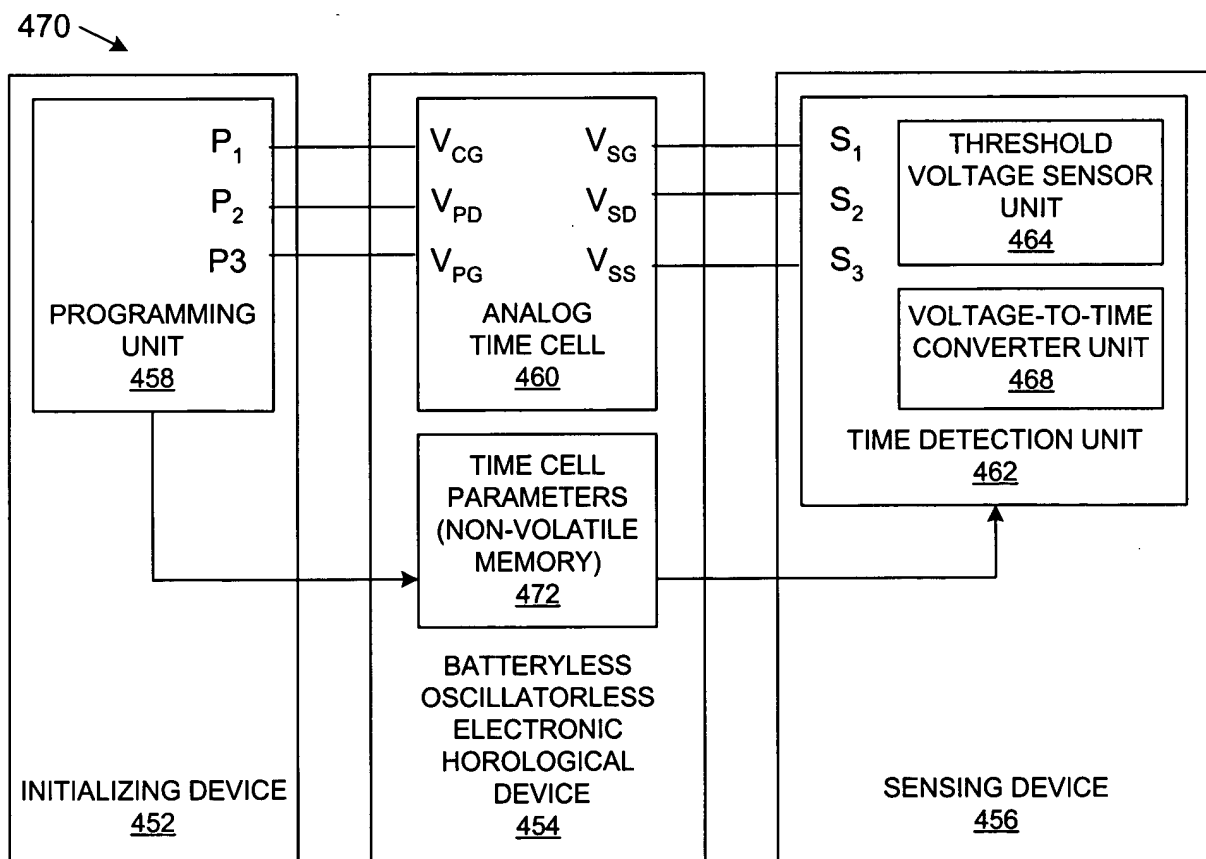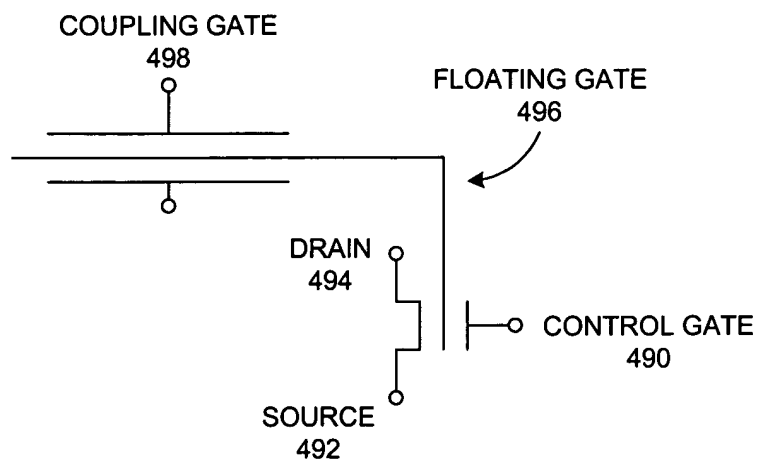Batteryless, oscillatorless, analog time cell usable as an horological device
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450 ⟍

PROGRAMMING
UNIT
458

P_1
P_2
P3

INITIALIZING DEVICE
452

V_{CG} V_{SG}
V_{PD} V_{SD}
V_{PG} V_{SS}

ANALOG
TIME CELL
460

BATTERYLESS
OSCILLATORLESS
ELECTRONIC
HOROLOGICAL
DEVICE
454

S_1
S_2
S_3

THRESHOLD
VOLTAGE SENSOR
UNIT
464

VOLTAGE-TO-TIME
CONVERTER UNIT
468

TIME DETECTION UNIT
462

SENSING DEVICE
456

Figure 4K

470 ⟍

PROGRAMMING
UNIT
458

P_1
P_2
P3

INITIALIZING DEVICE
452

V_{CG} V_{SG}
V_{PD} V_{SD}
V_{PG} V_{SS}

ANALOG
TIME CELL
460

TIME CELL
PARAMETERS
(NON-VOLATILE
MEMORY)
472

BATTERYLESS
OSCILLATORLESS
ELECTRONIC
HOROLOGICAL
DEVICE
454

S_1
S_2
S_3

THRESHOLD
VOLTAGE SENSOR
UNIT
464

VOLTAGE-TO-TIME
CONVERTER UNIT
468

TIME DETECTION UNIT
462

SENSING DEVICE
456

Figure 4L

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COUPLING GATE
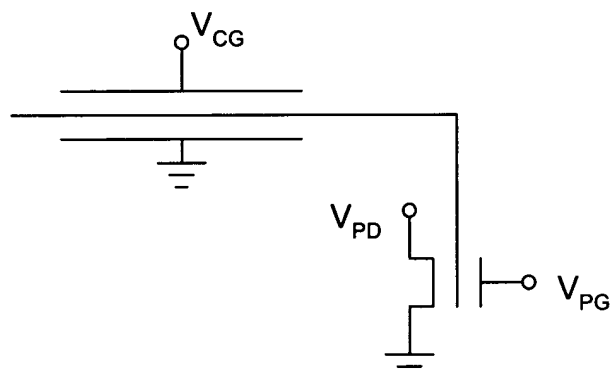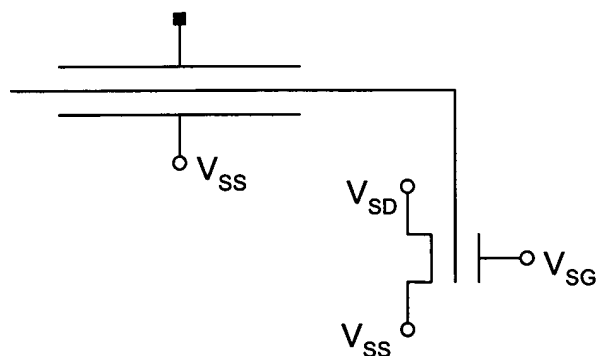498

FLOATING GATE
496

DRAIN
494

CONTROL GATE
490

SOURCE
492

Figure 4M

V_{CG}

V_{PD}

V_{PG}

Figure 4N

V_{SS}

V_{SD}

V_{SG}

V_{SS}

Figure 4O

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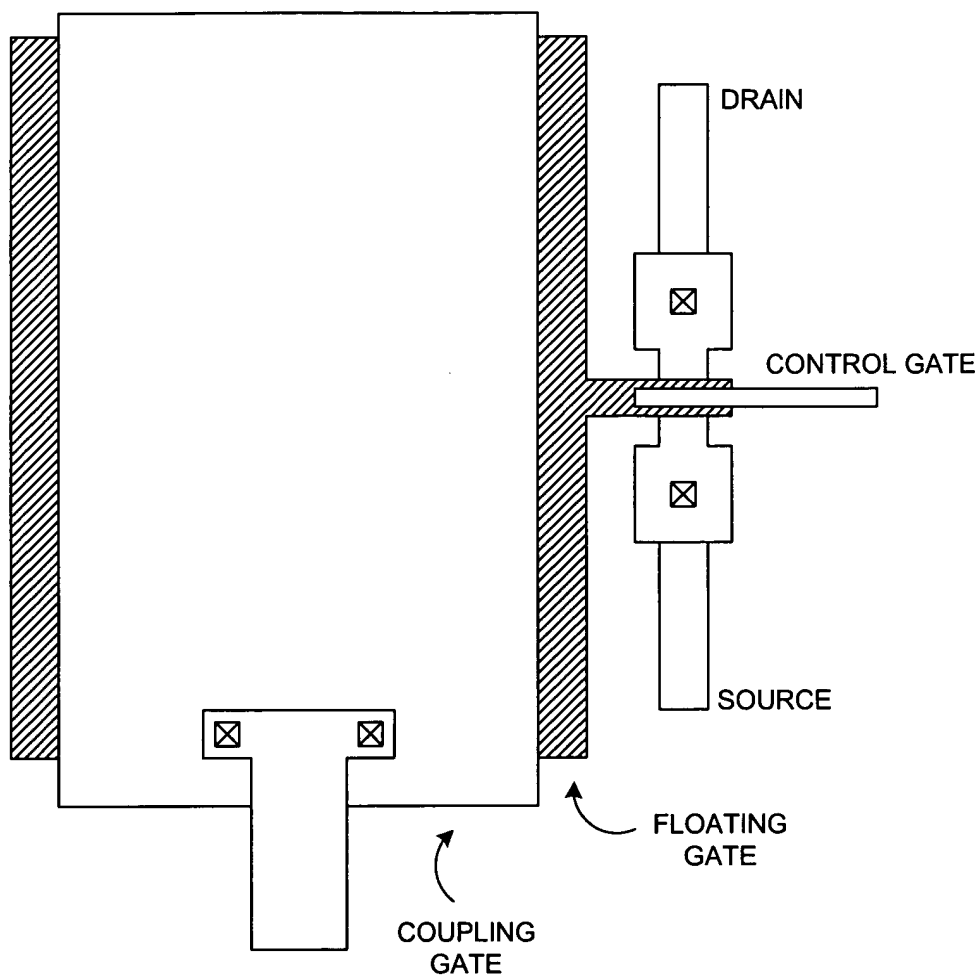
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Figure 4P